B. Tech.

Third Semester Theory Examination, 2011-12

DIGITAL LOGIC DESIGN

Time: 3 Hours  [Total Marks: 100]

Note: Attempt all questions as per directions given thereof.

Be precise in your answer.

Section-A

1. Attempt all subquestions: \(2 \times 10 = 20\)

(a) Represent the decimal number 5137 in (i) BCD,
    (ii) excess-3 code, (iii) 2421 code and (iv) a 6311 code.
(b) Express the Boolean function \( F(A, B, C) = A + \overline{B}C \) as a sum of minterms.

(c) Design a full adder using NAND gate.

(d) Design a 2-bit magnitude comparator using logic gates.

(e) Explain the difference between latch and flip-flop.

(f) What is the difference between serial and parallel transfer? Which transfer is faster one? Explain how to convert serial data to parallel? What type of register is needed?

(g) What is race around condition? Explain in brief.

(h) Implement the function:
\[
F = \overline{A}B + A\overline{B} + \overline{A}BCD + A\overline{BC} + AB + C
\]
using PLA.
(i) Explain the difference between EPROM and EEPROM. A certain memory has a capacity of 8 K x 16. How many bits are in each word? How many words are being stored?

(j) Explain how the ASM chart differs from conventional flow chart.

**Section-B**

2. Attempt all subquestions: 6 x 5 = 30

(a) Draw a NAND logic diagram that implements the complement of the following function:

\[ F(A, B, C, D) = \Sigma (0, 1, 2, 3, 4, 8, 9, 10, 11, 12). \]

(b) Implement a full adder with two 4 x 1 multiplexers.

(c) Show that the characteristic equation for the complement output of a JK flip-flop is:

\[ Q'(T+1) = J'Q' + KQ. \]
(d) Draw a PLA circuit to implement the functions:

\[
F_1 = \overline{AB} + \overline{AC} + \overline{ABC} \\
F_2 = (AB + AC + BC)
\]

(e) Differentiate synchronous and asynchronous sequential circuits. Explain the problem in asynchronous sequential circuits.

**Section-C**

3. Attempt all subquestions: 10\times5=50

(a) Design a Gray to BCD code converter using 1:16 demultiplexer (with active low output).

Or

Design a parity generator and checker operate using odd parity.

(b) What is the difference between decoder and encoder? Design a four input priority encoder with inputs as given table. Here \(D_0\) has the highest priority and \(D_3\) the lowest priority.

0109 (4)
Implement the following function using $16 \times 1$ MUX and $8 \times 1$ MUX:

$$F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 7, 8, 9, 11, 14, 15).$$

(c) Explain the difference among a truth table, a state table, a characteristic table and an excitation table. Also explain the difference among a Boolean equation, a state equation, a characteristic equation and a flip-flop input equation.
Or

Design a synchronous, recycling MOD-8, binary down counter with D flip-flop.

(d) Show the memory cycle timing waveform for the write and read operation. Assume a CPU clock of 50 MHz and memory cycle time of 50 ns.

Or

Draw an ASM chart for a MOD-6 counter with a reset input.

(e) An asynchronous sequential circuit is described by the excitation function \( Y = X_1X_2'(X_1' + X_2') \) and output function \( z = y \).

(i) Draw the logic diagram of circuit.
(ii) Derive the transition table and output map.
(iii) Obtain two-state flow table.
(iv) Describe in words the behaviour of circuit.
Or
What are the different types of hazards in asynchronous circuits? Draw the logic diagram of the POS expression \( Y = (X_1+X_2') (X_2'+X_3) \).
Show that there is a static-0 hazard when \( X_1 \) and \( X_3 \) are equal to 0 and \( X_2 \) goes from 0 to 1. Find the way to remove the hazard by adding one more OR gate.